# VNQ690SP-E

## QUAD CHANNEL HIGH SIDE DRIVER

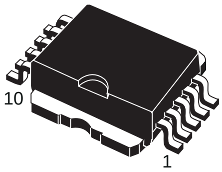
**Table 1. General Features**

| Type | $R_{DS(on)}$ | $I_{out}$ | $V_{CC}$ |
|---|---|---|---|
| VNQ690SP-E | 90mΩ (*) | 10A | 36V |

(*) Per each channel

- OUTPUT CURRENT PER CHANNEL: 10A
- CMOS COMPATIBLE INPUTS
- OPEN LOAD DETECTION (OFF STATE)
- UNDERVOLTAGE & OVERVOLTAGE SHUT- DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST: LOSS OF GROUND & LOSS OF $V_{CC}$
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

**Figure 1. Package**



PowerSO-10™

### DESCRIPTION

The VNQ690SP-E is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving resistive or inductive loads with one side connected to ground. This device has four independent channels.

Built-in thermal shut down and output current limitation protect the chip from over temperature and short circuit.

**Table 2. Order Codes**

| Package | Tube | Tape and Reel |
|---|---|---|
| PowerSO-10™ | VNQ690SP-E | VNQ690SPTR-E |

Note: (**) See application schematic at page 9

Rev. 1

**Figure 2. Block Diagram**

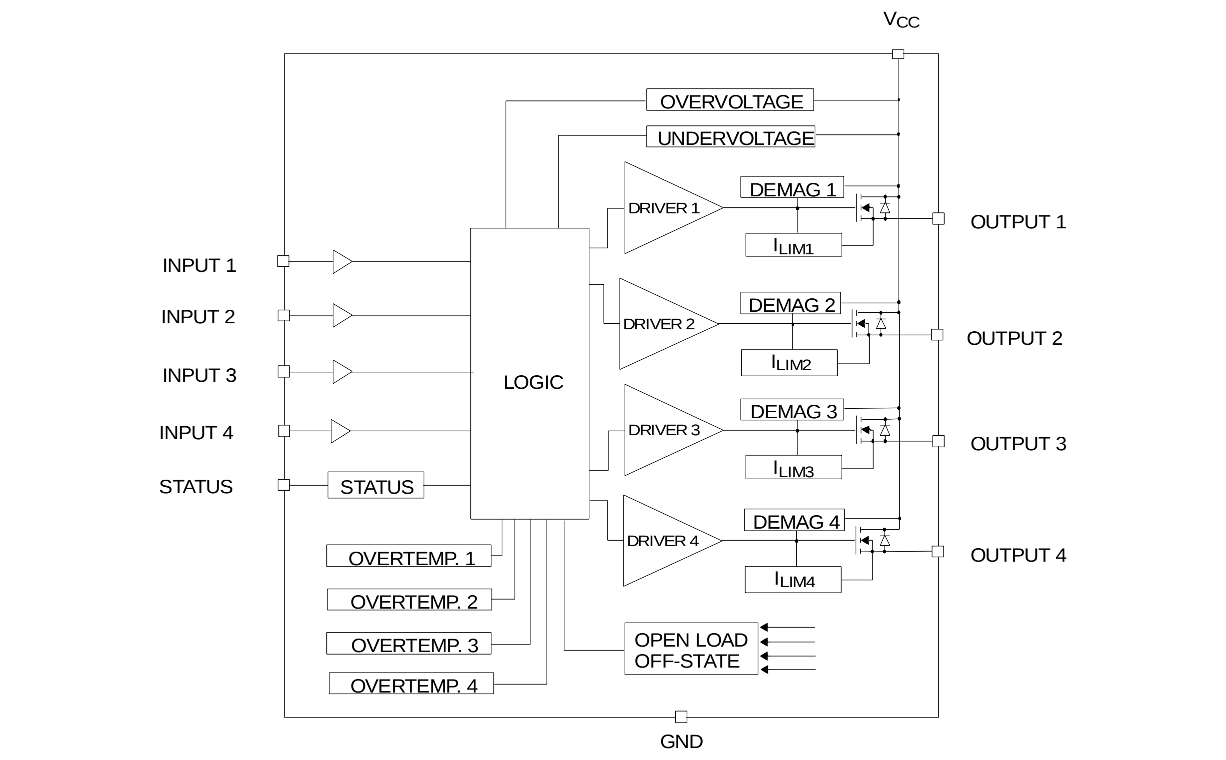
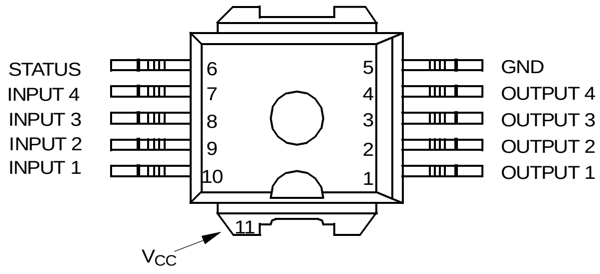



**Table 3. Absolute Maximum Ratings**

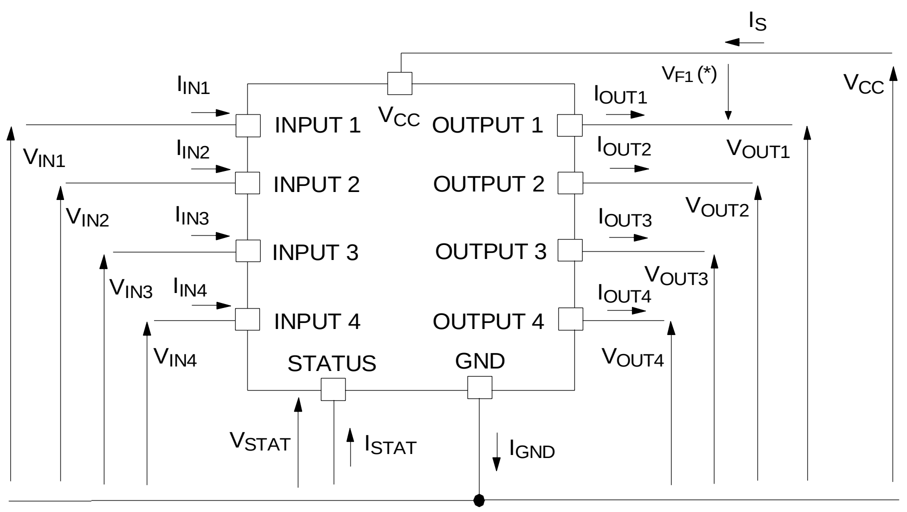
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage (continuous) | 41 | V |
| $-V_{CC}$ | Reverse supply voltage (continuous) | -0.3 | V |
| $I_{OUT}$ | Output current (continuous), per each channel | Internally limited | A |
| $I_R$ | Reverse output current (continuous), per each channel | -15 | A |
| $I_{IN}$ | Input current | +/- 10 | mA |
| $I_{STAT}$ | Status current | +/- 10 | mA |
| $I_{GND}$ | Ground current at $T_C \leq 25°C$ (continuous) | -200 | mA |
| $V_{ESD}$ | Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)<br>- INPUT<br>- STATUS<br>- OUTPUT<br>- $V_{CC}$ | <br>4000<br>4000<br>5000<br>5000 | <br>V<br>V<br>V<br>V |
| $P_{tot}$ | Power dissipation at $T_C=25°C$ | 78 | W |
| $E_{MAX}$ | Maximum Switching Energy<br>(L=0.38mH; $R_L=0Ω$; $V_{bat}=13.5V$; $T_{jstart}=150ºC$; $I_L=14A$) | 53 | mJ |
| $T_j$ | Junction operating temperature | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |

**Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins**




| Connection / Pin | Status | N.C. | Output | Input |
|---|---|---|---|---|
| Floating | X | X | X | X |
| To Ground | | X | | Through 10KΩ resistor |

**Figure 4. Current and Voltage Conventions**




(*) $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

**Table 4. Thermal Data**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case (MAX) per channel | 2 | | °C/W |
| $R_{tj\text{-}amb}$ | Thermal resistance junction-ambient (MAX) | 52 (1) | 37 (2) | °C/W |

Note: 1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35 µm thick)

Note: 2. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35 µm thick).

## ELECTRICAL CHARACTERISTICS

($V_{CC}$=6V up to 24V; -40°C<$T_j$<150°C unless otherwise specified)

**Table 5. Power** (Per each channel)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ (#) | Operating supply voltage | | 6 | 13 | 36 | V |
| $V_{USD}$ (#) | Undervoltage shutdown | | 3.5 | 4.6 | 6 | V |
| $V_{UVhyst}$ (#) | Undervoltage hysteresis | | 0.2 | | 1 | V |
| $V_{OV}$ (#) | Overvoltage shutdown | | 36 | | | V |
| $V_{OVhyst}$ (#) | Overvoltage hysteresis | | 0.25 | | | V |
| $I_S$ (#) | Supply current | Off state; $V_{IN}$=$V_{OUT}$=0V; $V_{CC}$=13.5V<br>Off state; $V_{IN}$=$V_{OUT}$=0V; $V_{CC}$=13.5V $T_j$=25°C<br>On state; $V_{IN}$=3.25V; 9V<$V_{CC}$<18V | | 12<br>12<br>6 | 40<br>25<br>12 | µA<br>µA<br>mA |
| $R_{ON}$ | On state resistance | $I_{OUT}$=1A; $T_j$=25°C; 9V<$V_{CC}$<18V<br>$I_{OUT}$=1A, $T_j$=150°C; 9V<$V_{CC}$<18V | | | 90<br>180 | mΩ<br>mΩ |
| $I_{L(off1)}$ | Off State Output Current | $V_{IN}$=$V_{OUT}$=0V | 0 | | 50 | µA |
| $I_{L(off2)}$ | Off State Output Current | $V_{IN}$=0V; $V_{OUT}$=3.5V | -75 | | 0 | µA |
| $I_{L(off3)}$ | Off State Output Current | $V_{IN}$=$V_{OUT}$=0V; $V_{CC}$=13V; $T_j$ =125°C | | | 5 | µA |
| $I_{L(off4)}$ | Off State Output Current | $V_{IN}$=$V_{OUT}$=0V; $V_{CC}$=13V; $T_j$ =25°C | | | 3 | µA |

Note: (#) Per device.

**Table 6. Protection** (see note 1)
(per each channel)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{TSD}$ | Shutdown temperature | | 150 | 170 | 200 | °C |
| $T_R$ | Reset temperature | | 135 | | | °C |
| $T_{hyst}$ | Thermal hysteresis | | 7 | 15 | 25 | °C |
| $I_{LIM}$ | DC Short circuit current | 9V<$V_{CC}$<36V<br>6V<$V_{CC}$<36V | 10 | 14 | 20<br>20 | A<br>A |
| $V_{demag}$ | Turn-off output voltage clamp | $I_{OUT}$=2A; $V_{IN}$=0V; L=6mH | $V_{CC}$-41 | $V_{CC}$-48 | $V_{CC}$-55 | V |
| $V_{STAT}$ | Status low output voltage | $I_{STAT}$=1.6mA | | | 0.5 | V |
| $I_{LSTAT}$ | Status leakage current | Normal operation; $V_{STAT}$=5V | | | 10 | µA |
| $C_{STAT}$ | Status pin input capacitance | Normal operation; $V_{STAT}$=5V | | | 25 | pF |
| $V_{SCL}$ | Status clamp voltage | $I_{STAT}$=1mA<br>$I_{STAT}$=-1mA | 6 | 6.8<br>-0.7 | 8 | V<br>V |

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

## ELECTRICAL CHARACTERISTICS (continued)

**Table 7. $V_{CC}$ - Output Diode**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_F$ | Forward on Voltage | $-I_{OUT}$=0.9A; $T_j$=150°C | | | 0.6 | V |

**Table 8. Switching** ($V_{CC}$=13V)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $R_L$=13Ω channels 1,2,3,4 | | 30 | | µs |
| $t_{d(off)}$ | Turn-off delay time | $R_L$=13Ω channels 1,2,3,4 | | 30 | | µs |
| $dV_{OUT}/dt_{(on)}$ | Turn-on voltage slope | $R_L$=13Ω channels 1,2,3,4 | | See relative diagram | | V/µs |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope | $R_L$=13Ω channels 1,2,3,4 | | See relative diagram | | V/µs |

**Table 9. Openload Detection** (off state) per each channel

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SDL}$ | Status Delay | See Figure 1 (Openload detection reading must be performed after $T_{DOL}$). | | | 20 | µs |
| $V_{OL}$ | Openload Voltage Detection Threshold | $V_{IN}$=0V | 1.5 | 2.5 | 3.5 | V |
| $T_{DOL}$ | Openload Detection Delay at Turn Off | $V_{CC}$=18V | | | 300 | µs |

**Table 10. Logic Input**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Level Voltage | | | | 1.25 | V |
| $V_{IH}$ | Input High Level Voltage | | 3.25 | | | V |
| $V_{HYST}$ | Input Hysteresis Voltage | | 0.5 | | | V |
| $I_{IH}$ | Input high level voltage | $V_{IN}$=3.25V | | | 10 | µA |
| $I_{IL}$ | Input Current | $V_{IN}$=1.25V | 1 | | | µA |
| $V_{ICL}$ | Input Clamp Voltage | $I_{IN}$=1mA | 6 | 6.8 | 8 | V |
| | | $I_{IN}$=-1mA | | -0.7 | | V |

**Figure 5. Status Timing Waveforms**

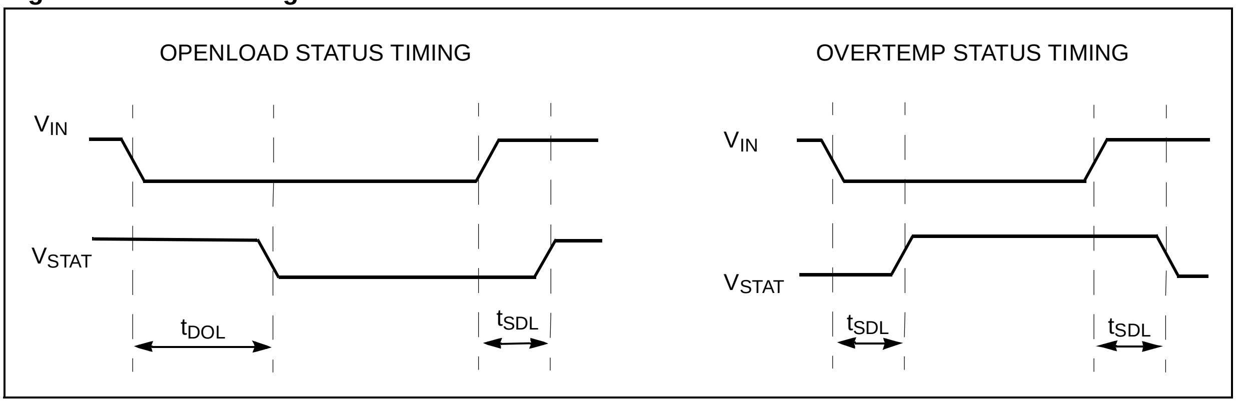
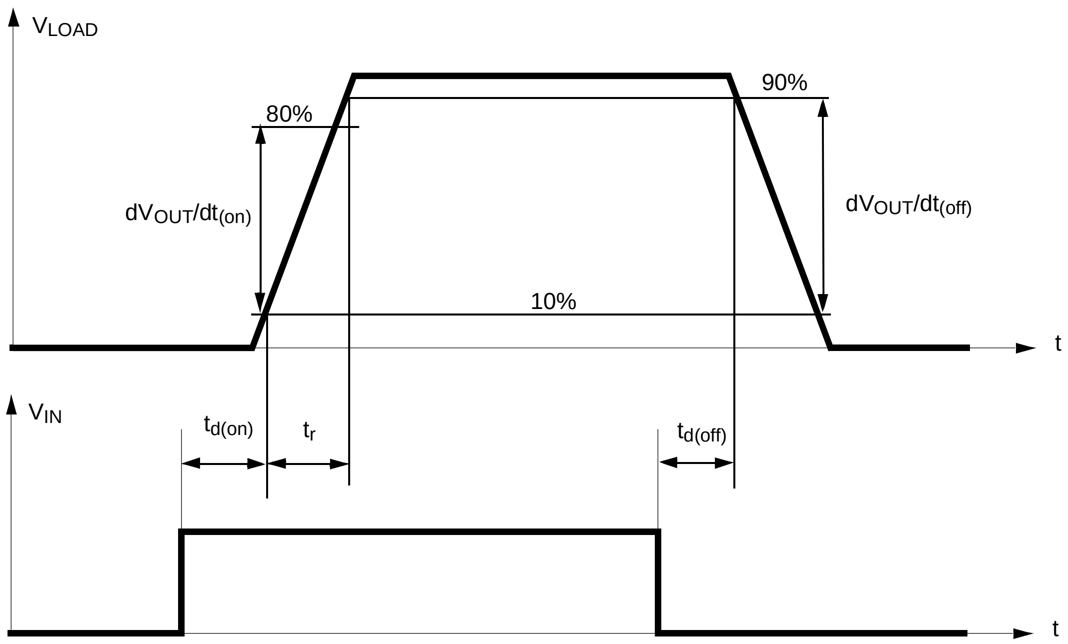


**Table 11. Truth Table** (Per each channel)

| CONDITIONS | INPUT | OUTPUT | SENSE |
|---|---|---|---|
| Normal Operation | L<br>H | L<br>H | H<br>H |
| Overtemperature | L<br>H | L<br>L | H<br>L |
| Undervoltage | L<br>H | L<br>L | X<br>X |
| Overvoltage | L<br>H | L<br>L | H<br>H |
| Current Limitation | L<br>H | L<br>X | H<br>H |
| Output Voltage > $V_{OL}$ | L<br>H | H<br>H | L<br>H |

**Figure 6. Switching Characteristics**



## Table 12. Electrical Transient Requirements

| ISO T/R 7637/1<br>Test Pulse | TEST LEVELS | | | | |
|---|---|---|---|---|---|
| | I | II | III | IV | Delays and Impedance |
| 1 | -25 V | -50 V | -75 V | -100 V | 2 ms 10 Ω |
| 2 | +25 V | +50 V | +75 V | +100 V | 0.2 ms 10 Ω |
| 3a | -25 V | -50 V | -100 V | -150 V | 0.1 µs 50 Ω |
| 3b | +25 V | +50 V | +75 V | +100 V | 0.1 µs 50 Ω |
| 4 | -4 V | -5 V | -6 V | -7 V | 100 ms, 0.01 Ω |

| ISO T/R 7637/1 Test Pulse | Test Levels Result | | | |
|---|---|---|---|---|
| | I | II | III | IV |
| 1 | C | C | C | C |
| 2 | C | C | C | C |
| 3a | C | C | C | C |
| 3b | C | C | C | C |
| 4 | C | C | C | C |
| 5 | C | E | E | E |

| CLASS | CONTENTS |
|---|---|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device. |

**Figure 7. Waveforms**

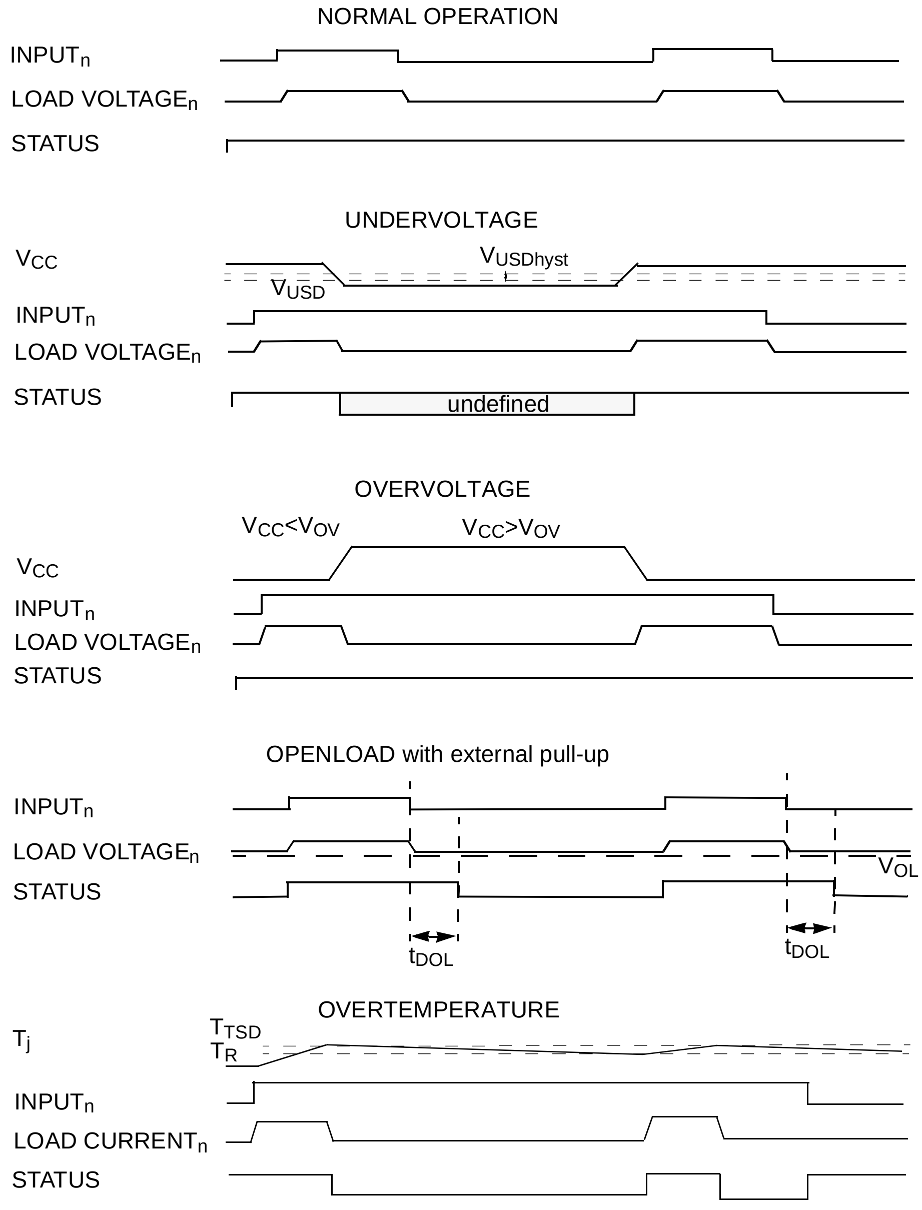
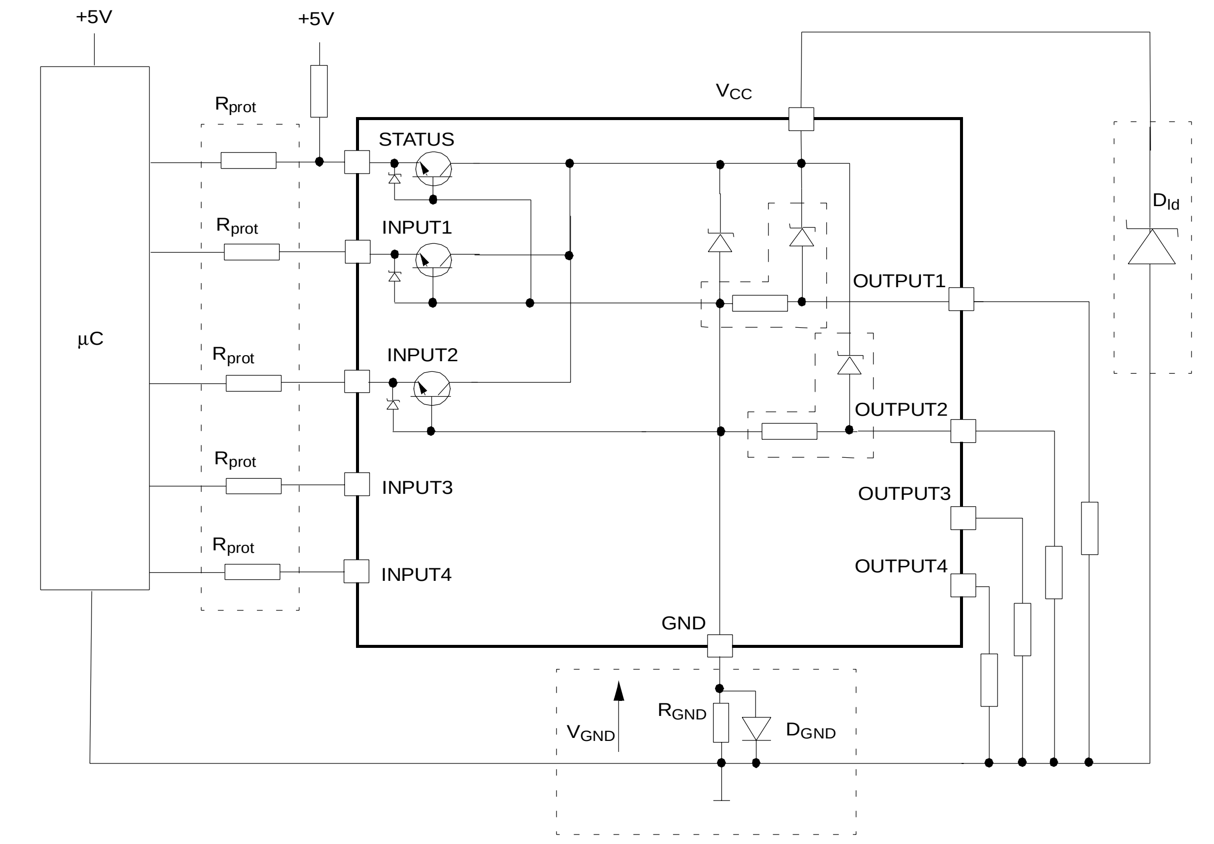


**Figure 8. Application Schematic**




Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

## GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line ($R_{GND}$ only). This can be used with any type of load.

The following is an indication on how to dimension the $R_{GND}$ resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in $R_{GND}$ (when $V_{CC}$<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the $R_{GND}$ will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same $R_{GND}$.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode ($D_{GND}$) in the ground line.

A resistor ($R_{GND}$=1kΩ) should be inserted in parallel to $D_{GND}$ if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≃600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## LOAD DUMP PROTECTION

$D_{ld}$ is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds $V_{CC}$ max DC rating. The same applies if the device will be subject to transients on the $V_{CC}$ line that are greater than the ones shown in the ISO T/R 7637/1 table.

## μC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the $V_{CC}$ line, the control pins will be pulled negative. ST suggests to insert a resistor ($R_{prot}$) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For $V_{CCpeak}$= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$5k\Omega \leq R_{prot} \leq 65k\Omega$.

Recommended $R_{prot}$ value is 10kΩ.

**Figure 9. Off State Output Current**

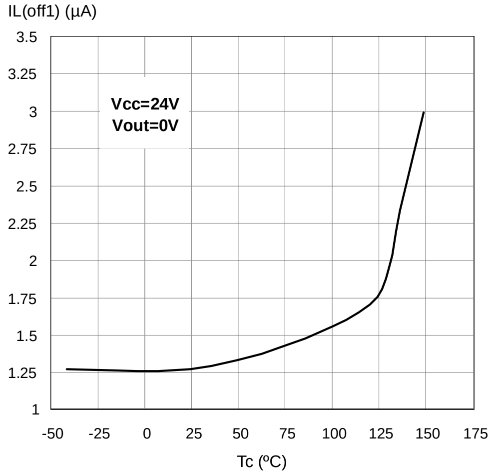



**Figure 12. High Level Input Current**

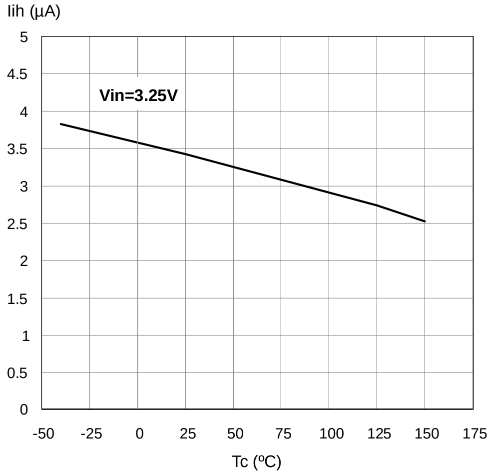



**Figure 10. Input High Level**

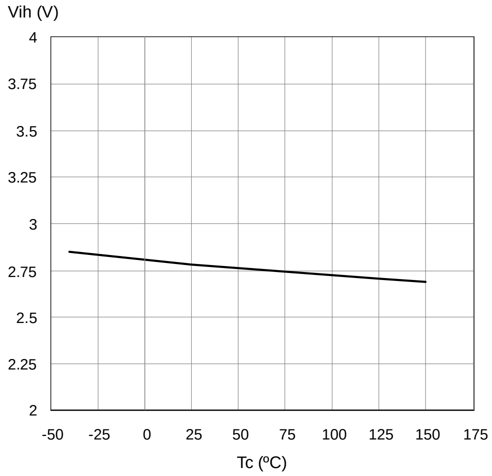



**Figure 13. Input Low Level**

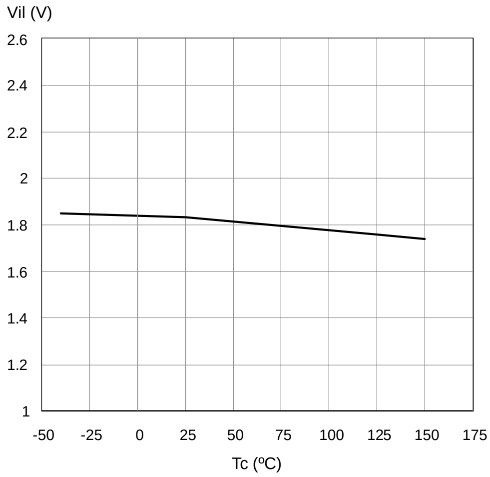



**Figure 11. Input Clamp Voltage**

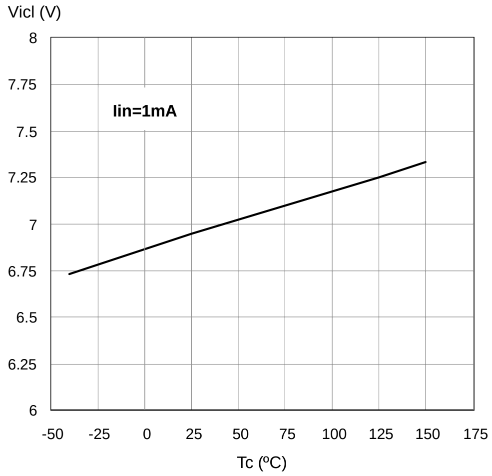



**Figure 14. Input Hysteresis Voltage**

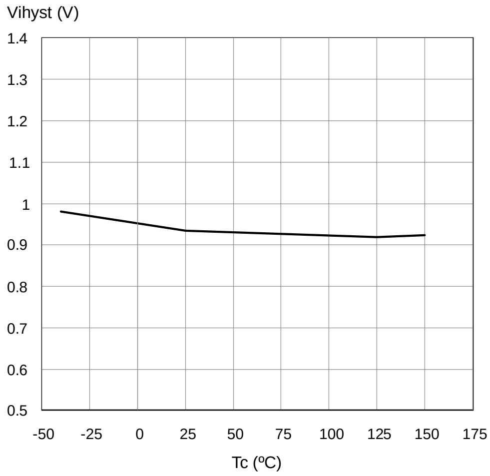


**Figure 15. Overvoltage Shutdown**

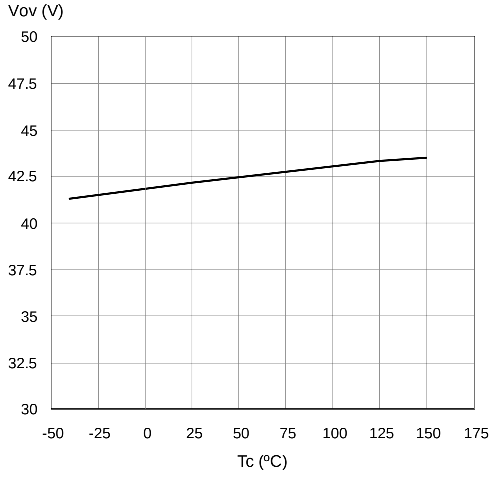



**Figure 16. Turn-on Voltage Slope**

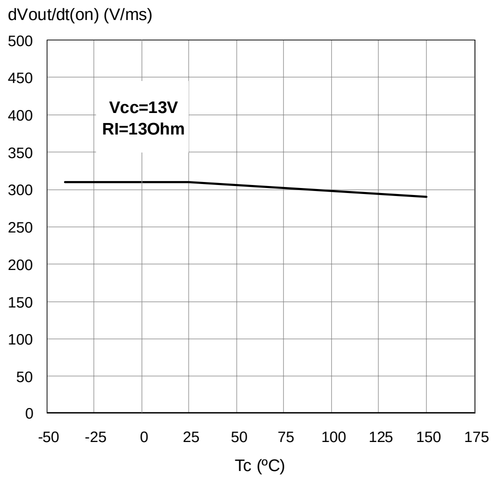



**Figure 17. $I_{LIM}$ Vs $T_{case}$**

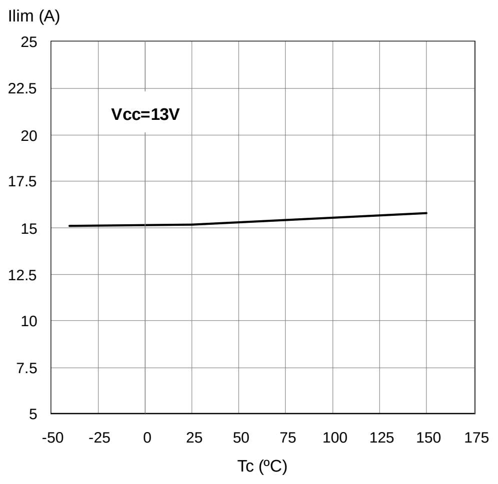



**Figure 18. Openload Off State Detection Threshold**

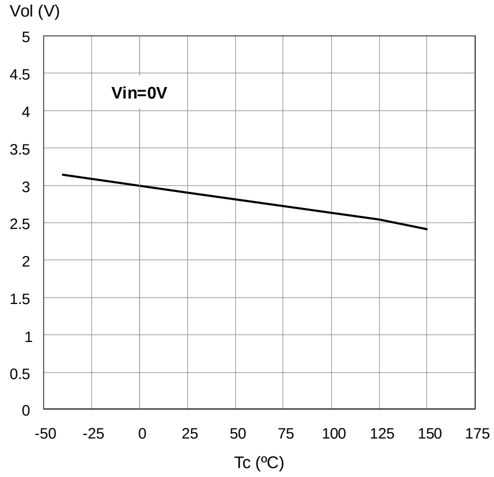



**Figure 19. Turn-off Voltage Slope**

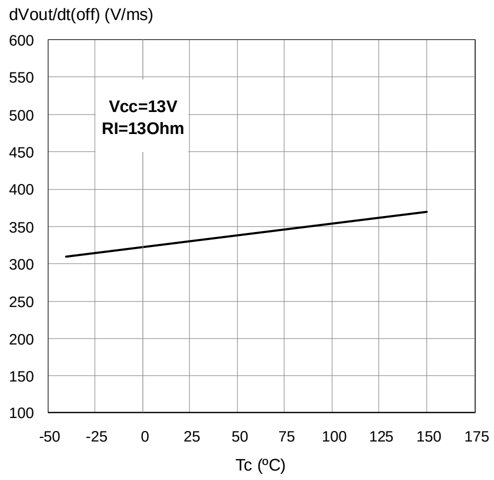



**Figure 20. On State Resistance Vs $V_{CC}$**

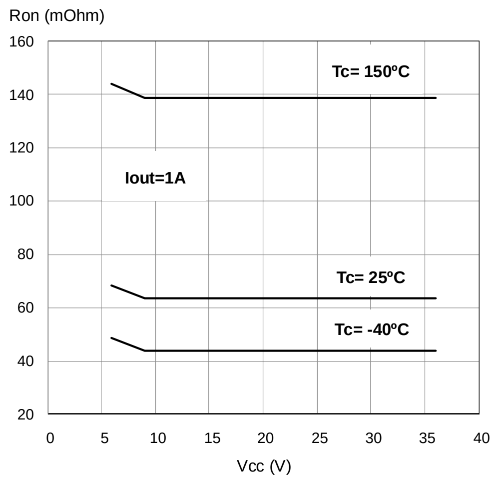


**Figure 21. On State Resistance Vs $T_{case}$**

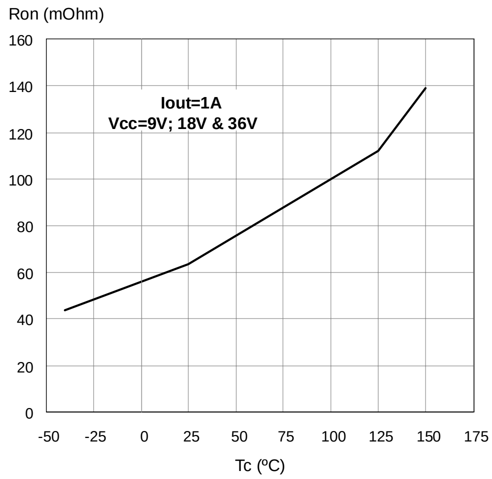



**Figure 23. Status Clamp Voltage**

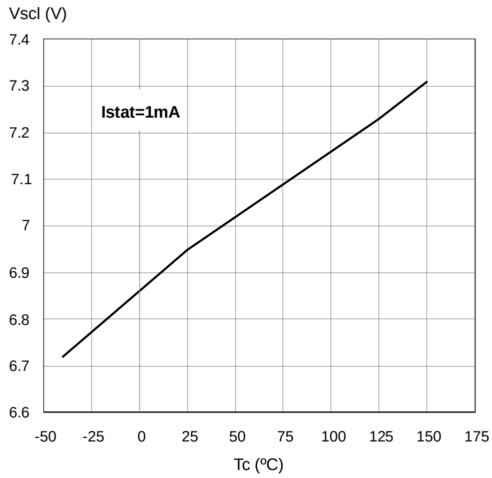



**Figure 22. Status Leakage Current**

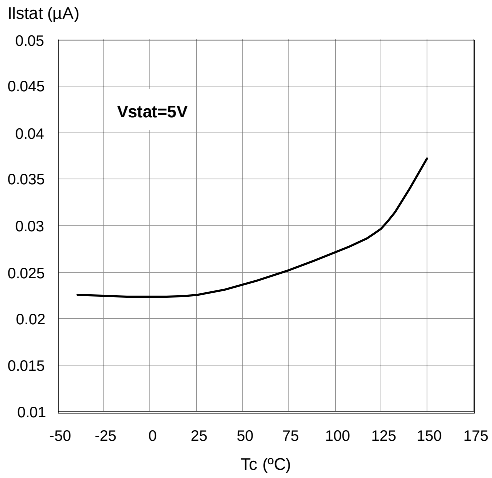



**Figure 24. Status Low Output Voltage**

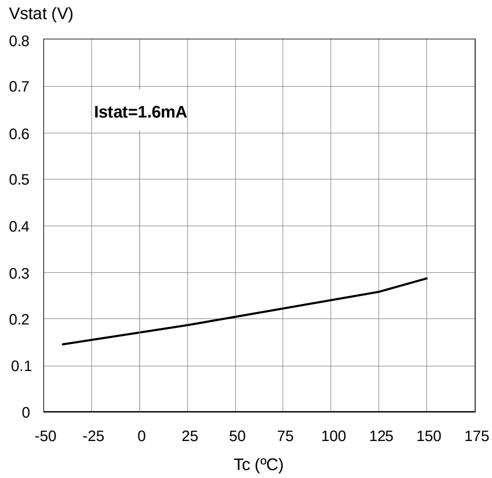
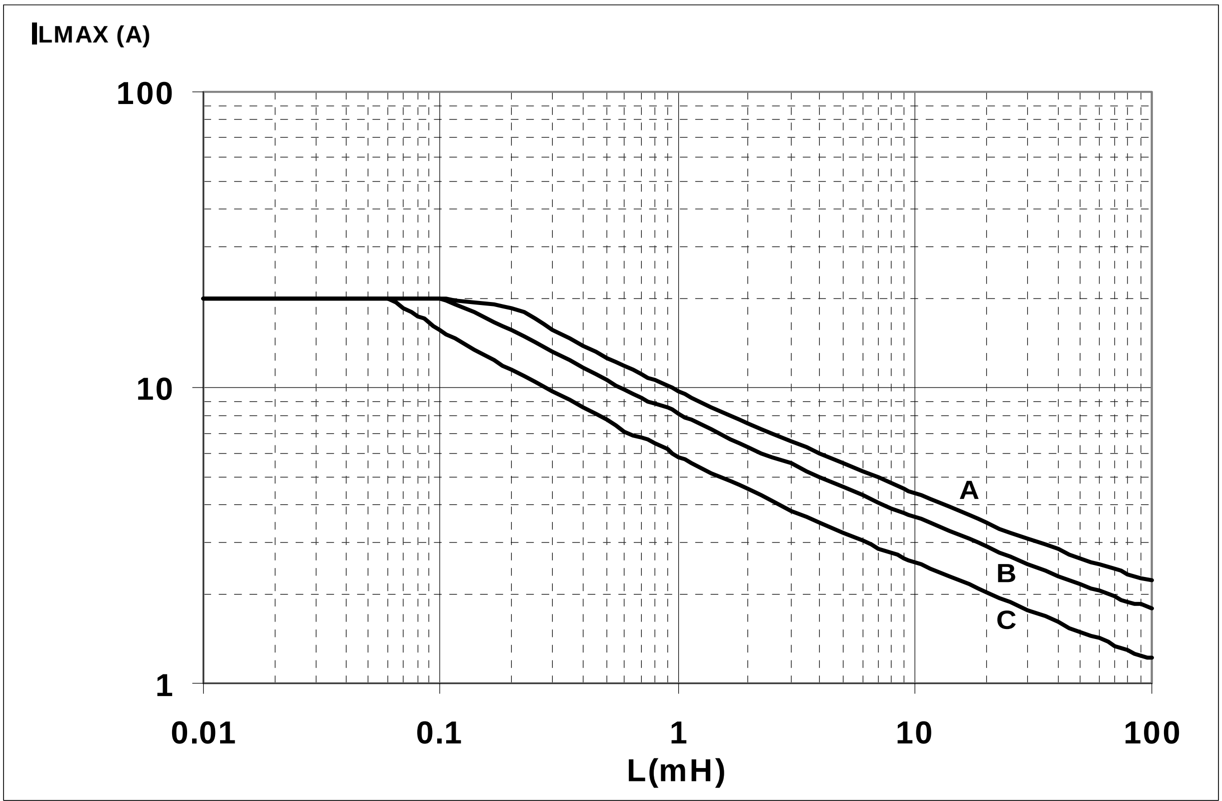


**Figure 25. Maximum turn off current versus load inductance**

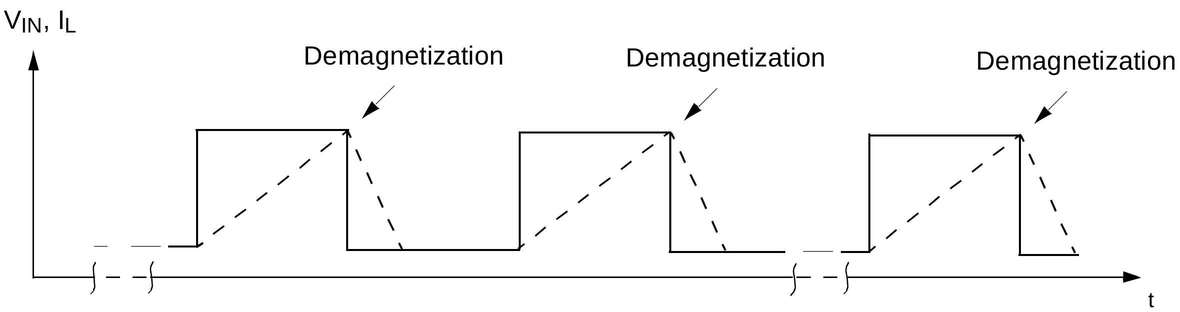



A = Single Pulse at $T_{Jstart}$=150ºC
B= Repetitive pulse at $T_{Jstart}$=100ºC
C= Repetitive Pulse at $T_{Jstart}$=125ºC

Conditions:
$V_{CC}$=13.5V

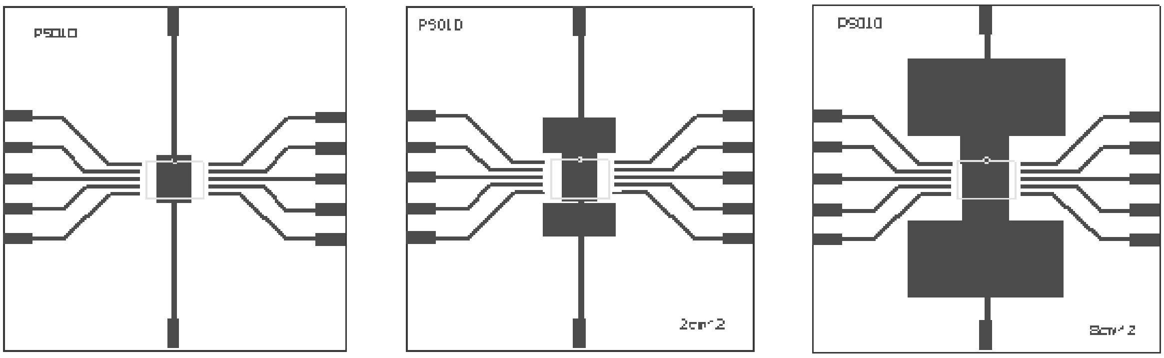
Values are generated with $R_L$=0Ω

In case of repetitive pulses, $T_{jstart}$ (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



## PowerSO-10™ Thermal Data

**Figure 26. PowerSO-10™ PC Board**




Layout condition of $R_{th}$ and $Z_{th}$ measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to 8cm$^2$).

**Figure 27. $R_{thj-amb}$ Vs PCB copper area in open box free air condition**

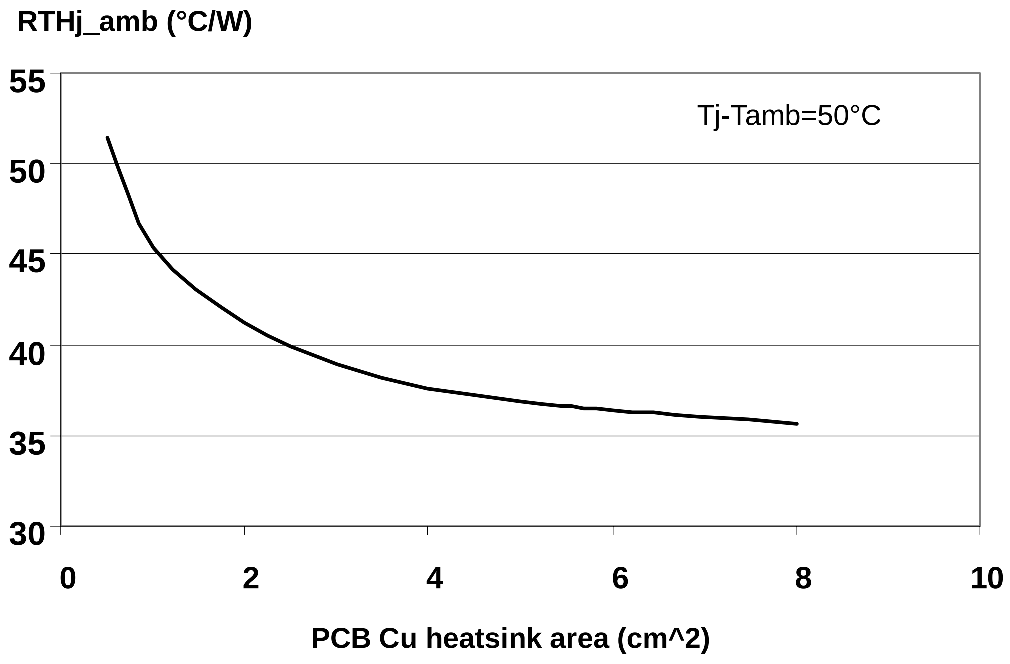


**Figure 28. PowerSO-10 Thermal Impedance Junction Ambient Single Pulse**

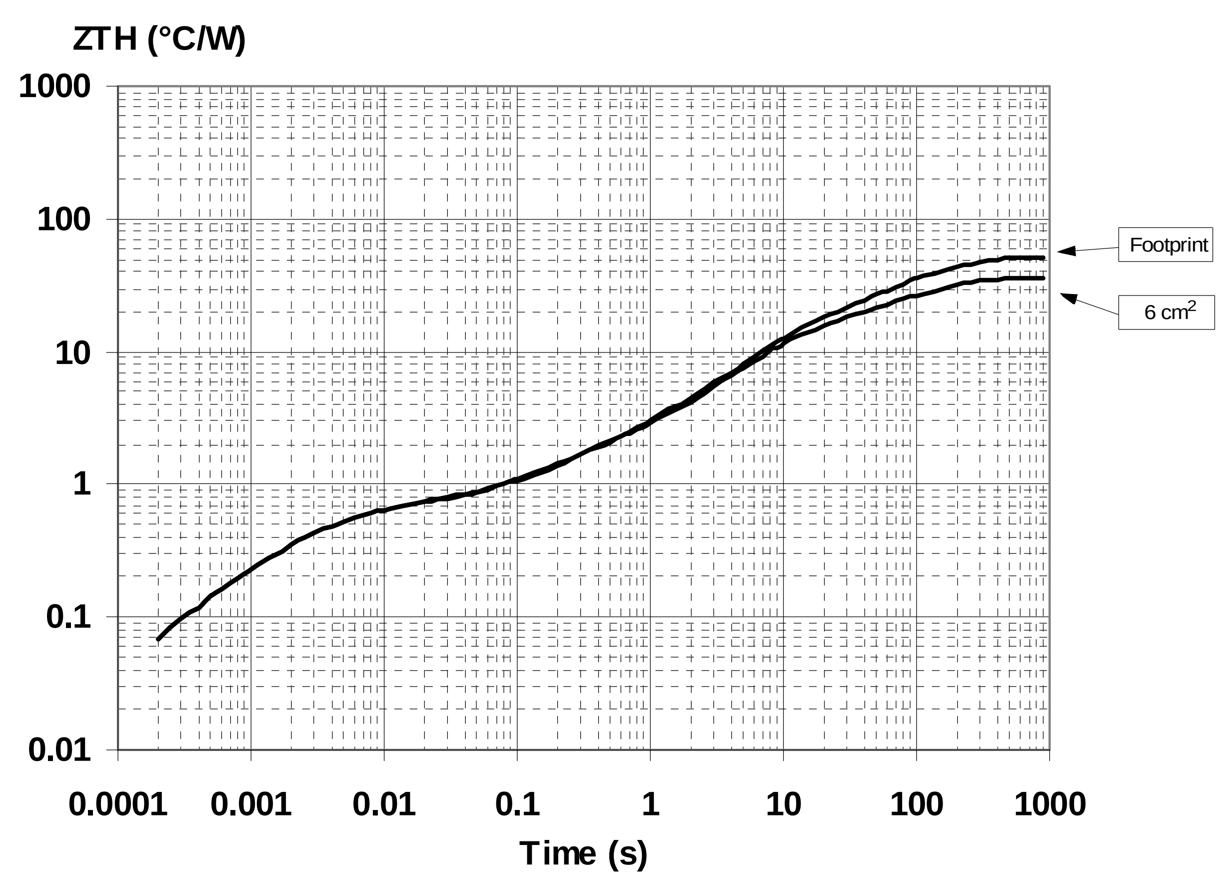
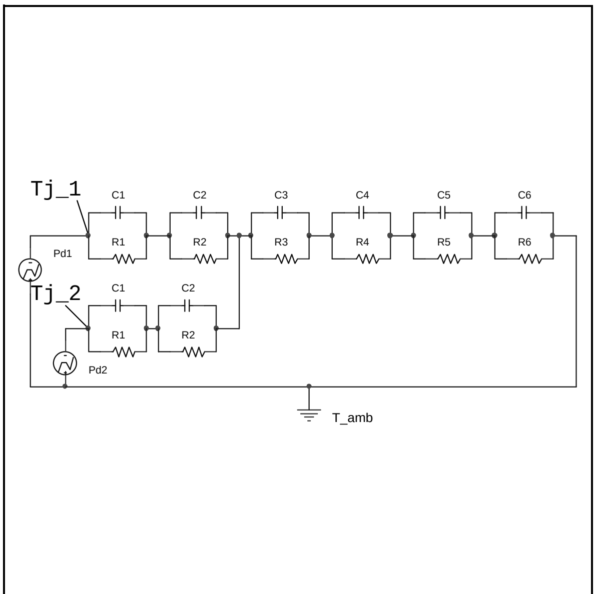



**Figure 29. Thermal fitting model of a double channel HSD in PowerSO-10**




**Pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

**Table 13. Thermal Parameter**

| Area/island ($cm^2$) | Footprint | 6 |
|---|---|---|
| R1 (°C/W) | 0.05 | |
| R2 (°C/W) | 0.3 | |
| R3( °C/W) | 0.3 | |
| R4 (°C/W) | 0.8 | |
| R5 (°C/W) | 12 | |
| R6 (°C/W) | 37 | 22 |
| C1 (W.s/°C) | 0.001 | |
| C2 (W.s/°C) | 5.00E-03 | |
| C3 (W.s/°C) | 0.02 | |
| C4 (W.s/°C) | 0.3 | |
| C5 (W.s/°C) | 0.75 | |
| C6 (W.s/°C) | 3 | 5 |

## PACKAGE MECHANICAL

### Table 14. PowerSO-10™ Mechanical Data

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 3.35 | | 3.65 |
| A (*) | 3.4 | | 3.6 |
| A1 | 0.00 | | 0.10 |
| B | 0.40 | | 0.60 |
| B (*) | 0.37 | | 0.53 |
| C | 0.35 | | 0.55 |
| C (*) | 0.23 | | 0.32 |
| D | 9.40 | | 9.60 |
| D1 | 7.40 | | 7.60 |
| E | 9.30 | | 9.50 |
| E2 | 7.20 | | 7.60 |
| E2 (*) | 7.30 | | 7.50 |
| E4 | 5.90 | | 6.10 |
| E4 (*) | 5.90 | | 6.30 |
| e | | 1.27 | |
| F | 1.25 | | 1.35 |
| F (*) | 1.20 | | 1.40 |
| H | 13.80 | | 14.40 |
| H (*) | 13.85 | | 14.35 |
| h | | 0.50 | |
| L | 1.20 | | 1.80 |
| L (*) | 0.80 | | 1.10 |
| a | 0º | | 8º |
| α (*) | 2º | | 8º |

Note: (*) Muar only POA P013P

### Figure 30. PowerSO-10™ Package Dimensions

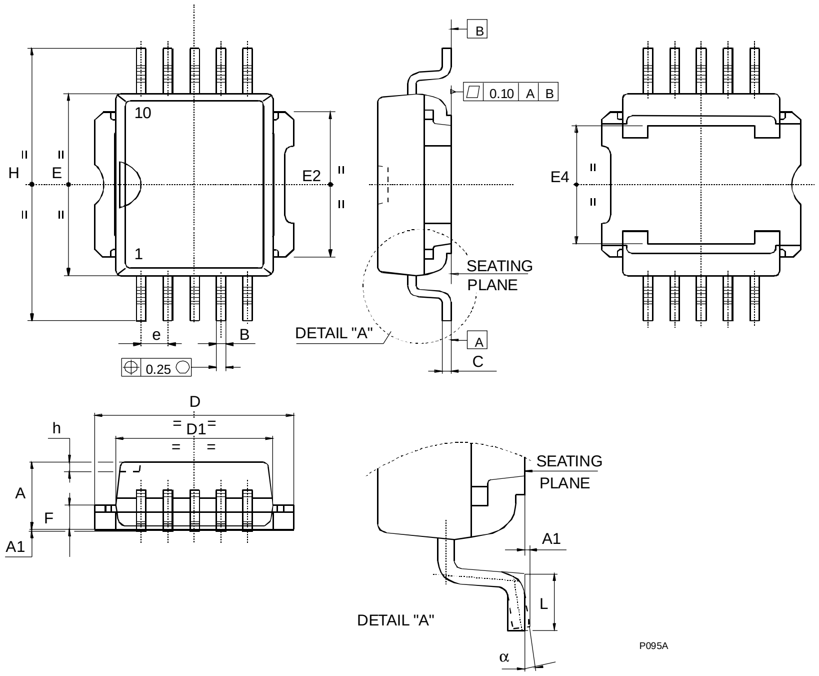
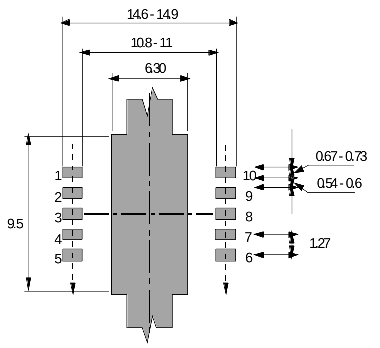
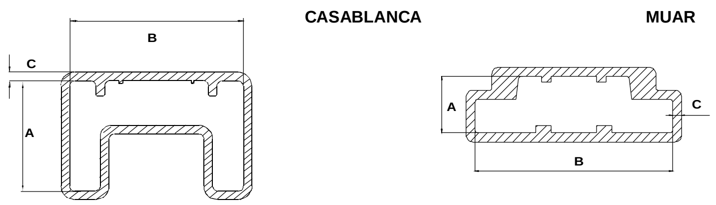


**Figure 31.** PowerSO-10™ **Suggested Pad Layout And Tube Shipment (No Suffix)**

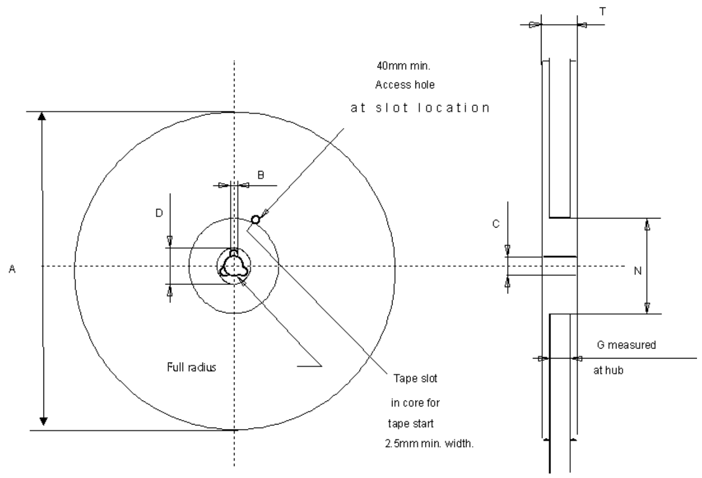



All dimensions are in mm.

| | Base Q.ty | Bulk Q.ty | Tube length (± 0.5) | A | B | C (± 0.1) |
|---|---|---|---|---|---|---|
| **Casablanca** | 50 | 1000 | 532 | 10.4 | 16.4 | 0.8 |
| **Muar** | 50 | 1000 | 532 | 4.9 | 17.2 | 0.8 |

**Figure 32. Tape And Reel Shipment (suffix "TR")**




## REEL DIMENSIONS

| | |
|---|---|
| **Base Q.ty** | 600 |
| **Bulk Q.ty** | 600 |
| **A (max)** | 330 |
| **B (min)** | 1.5 |
| **C (± 0.2)** | 13 |
| **F** | 20.2 |
| **G (+ 2 / -0)** | 24.4 |
| **N (min)** | 60 |
| **T (max)** | 30.4 |

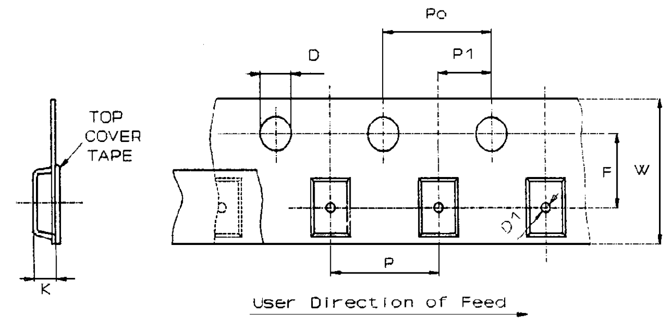
All dimensions are in mm.

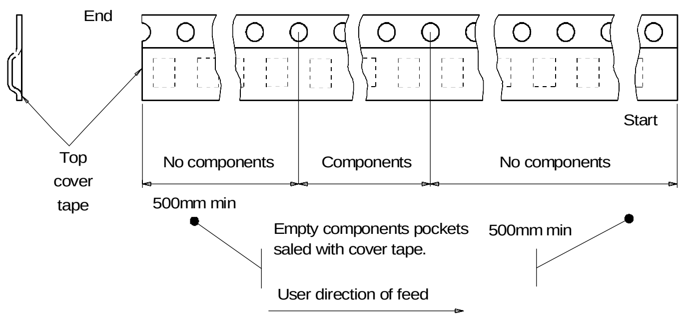
## TAPE DIMENSIONS

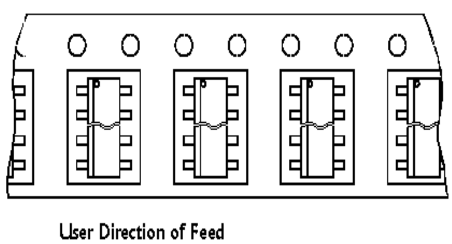
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|---|---|---|
| **Tape width** | **W** | 24 |
| **Tape Hole Spacing** | **P0 (± 0.1)** | 4 |
| **Component Spacing** | **P** | 24 |
| **Hole Diameter** | **D (± 0.1/-0)** | 1.5 |
| **Hole Diameter** | **D1 (min)** | 1.5 |
| **Hole Position** | **F (± 0.05)** | 11.5 |
| **Compartment Depth** | **K (max)** | 6.5 |
| **Hole Spacing** | **P1 (± 0.1)** | 2 |

All dimensions are in mm.



## REVISION HISTORY

| Date | Revision | Description of Changes |
|---|---|---|
| Oct. 2004 | 1 | - First Issue. |